Demonstrated Advanced Photonic Integration: Delivering Optical Interconnect at Scale

Disaggregation Manufacturing Organization, Intel Corporation, New Mexico, USA

Randal Appleton
Email: randal.s.appleton@intel.com

In this talk, we present Intel's latest advancements in silicon photonics integration. Integration occurs in three distinct arenas including on-die, on-package, and within-system. An advanced silicon photonics portfolio allows complex photonic integrated circuit fabrication at volume. Advanced packaging leadership unlocks cost-effective performance scaling. These technologies in turn allow new, resource efficient communication architectures. Demonstrated results in each area will be shared.

Short Bio: Dr. Randal Appleton is a Principal Engineer at Intel Corporation. He manages silicon photonics process architecture and new product integration for Intel's 300mm silicon photonics fabrication line where he is responsible for assessing photonics product needs against fab process capability, process requirements for new photonic device blocks, and timely development of new nodes to industry quality standards.

Randal started his Intel career as a process engineer for CMOS logic nodes before moving into silicon photonics, where he brought up Intel's first single crystal Ge deposition process for photodetection applications and matured the heterogeneous hybrid laser process to launch the industry-leading high volume silicon photonics platform used to ship >8 million transceivers and >32M integrated lasers.

Randal received his B.S. in Physics from Arizona State University, his M.S. in Physics from the University of Illinois at Urbana-Champaign, and his Ph.D. in Materials Science from the University of Illinois at Urbana-Champaign where he studied epitaxial thin film growth.